Application Note 1070-212

Case Study: A probe design enabling
ESD-sensitive device measurements in a PPMS

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Introduction

Studies of the current-voltage characteristics in materials often require device fabrication that incorporates features susceptible to damage from electrostatic discharge (ESD). Examples include insulated gate, point contact and tunneling magnetoresistance devices[1,2]. A common characteristic of device components sensitive to ESD is a highly resistive channel with no parallel resistive or junction-like path that can discharge static electricity as it is building up[3]. After experiencing ESD damage to insulated gate and point contact devices during sample puck installation in the Quantum Design PPMS we were motivated to develop a probe that would prevent ESD damage. Here we report on the construction of a probe that prevents ESD during sample installation and on the measurement of ESD sensitive devices made in our lab. It should be pointed out that there are many possible designs that address charge-sensitive sample measurements and this note describes just one of those.

1. S. M. Sze, K. K. Ng, *Physics of Semiconductor Devices* 3rd edition, Hoboken: John Wiley and Sons, Inc. 2007

2. A. Wallash, J. Hillman, M. Sharma, S. X. Wang, IEEE Transactions on Magnetics, Vol. 36, No. 5, September 2000

3. P. Horowitz, W. Hill, The Art of Electronics 2nd edition, Cambridge: Cambridge University Press 1989

Probe Design

Figure 1a-d shows the probe with critical elements labeled. We have incorporated design features to allow an installed device to maintain a single electrical ground during installation and measurements in the PPMS sample chamber. The probe avoids using the PPMS sample chamber wiring by routi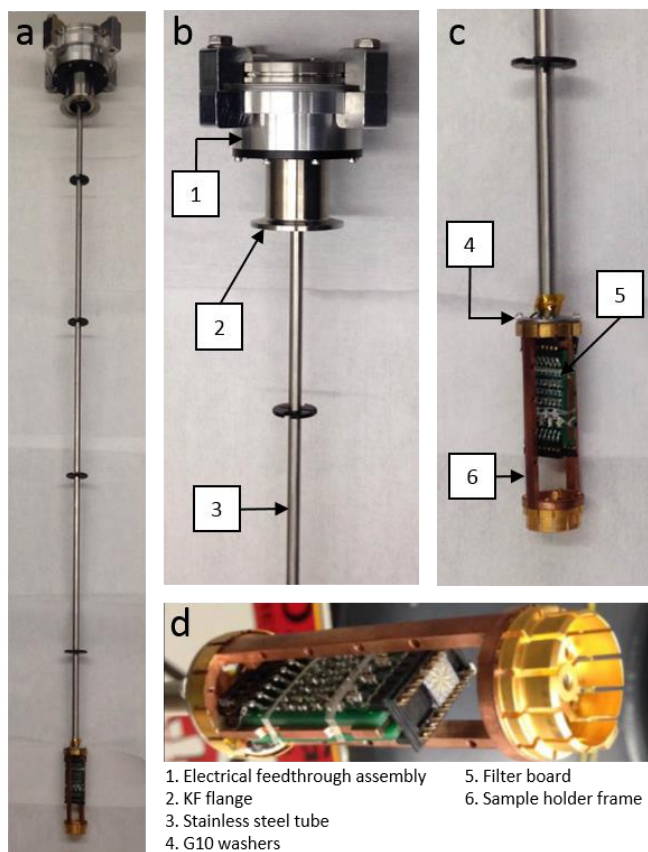ng the sample wiring through the electrical feedthrough assembly. The electrical feedthrough assembly includes a 25 pin D-sub vacuum feedthrough. On the vacuum side, 16 leads are provided by 8 twisted pair manganin cryogenic wires running from the D-sub connector through the stainless steel tube and connecting to two filter boards that hold a 16 pin DIP chip carrier on which a sample can be mounted. This wiring design allows the device to be connected to measurement electronics and an analog ground while the probe is outside of the PPMS sample chamber. The path to the electronics and analog ground is not broken during probe installation into the PPMS sample chamber.

R1: 820 Ω, R-EU-R0402, SUSUMU RR0510P-821-D
C1: 4700 pF, C-EU-C0603, TDK Corp C1608C0G1H472J080AA
R2: 1200 Ω, R-EU-R0402, SUSUMU RR0510P-122-D
C2: 22 nF, C-EU-C0603, TDK Corp CEU3E2X7R1H223K080AE
U1: 1.8 MHz low pass pi-filter Minicircuits LFCN-80

Figure 2. Figure 2. A schematic of the filters incorporated into each of the 16 leads. The component values, packaging and manufacturer part number are listed below the schematic.

1. Electrical feedthrough assembly
2. KF flange
3. Stainless steel tube
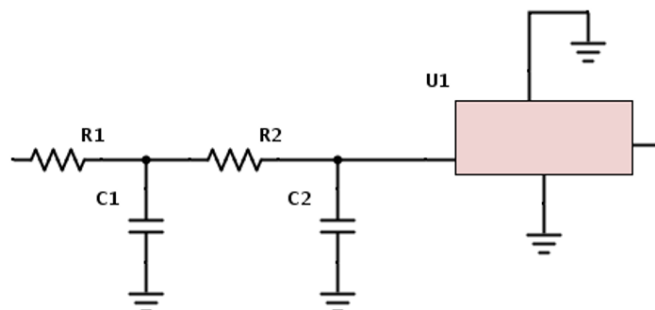4. G10 washers
5. Filter board
6. Sample holder frame

Figure 1. (a) A probe designed for measurements on ESD-sensitive devices (b) The portion of the probe providing electrical feedthroughs from atmosphere into the PPMS sample space under vacuum (c) The portion of the probe at which a sample on a 16 pin DIP chip can be mounted.

Furthermore, the probe and sample ground may be isolated from the chamber ground. The chamber is electrically connected to the KF flange and the sample holder frame. However, the KF flange is isolated from the probe by rubber seals and the sample holder frame is isolated from the probe by G10 washers. Therefore, the electrical feedthrough assembly, stainless steel tube and filter boards can be connected to a ground isolated from the chamber ground. Using an isolated ground allows shielding of the sample wiring from capacitive coupling to the chamber ground.

Figure 2 shows a schematic of the filters incorporated into each of the 16 leads. The filtering is not necessary for protection against ESD, but was incorporated to reduce high frequency noise at the sample.

Temperature Calibration

The temperature at the sample was calibrated using a LakeShore model CX-1050-SD Cernox temperature sensor. With helium exchange gas in the sample space we found the temperature measured by the Cernox temperature sensor to match the PPMS sample thermometer temperature over the range 2 Kelvin to 300 Kelvin. A small amount of hysteresis is observed during temperature cycling with a heating or cooling rate of 3 degrees Kelvin per minute. Without helium exchange gas in the sample space we found the temperature measured by the Cernox temperature sensor at the sample could not reach the base temperature of the PPMS. We believe a modification to the probe design that would increase thermal conduction between the probe and wiring with the cooling annulus could allow for operation down to 2 Kelvin under high vacuum conditions. The measurements discussed in the remainder of this application note were taken with helium exchange gas in the sample space.

Successful measurements of ESD-sensitive devices

We have successfully used the probe to measure ESD-sensitive insulating gate and point contact devices. Figure 3 shows the conductance as a function of gate voltage of a quantum point contact (QPC) fabricated over a GaAs/AlGaAs heterostructure hosting a two-dimensional electron gas (2DEG) measured on our probe using a 4-point configuration. Depletion of the 2DEG beneath the split gates occurs at approximately -0.2 V. The conductance through the QPC approaches zero at approximately -1.22 V. Similar devices have suffered from failure by ESD during sample insertion into the PPMS sample space using standard PPMS pucks. We have not observed a failure during sample insertion into the PPMS sample space using our probe.
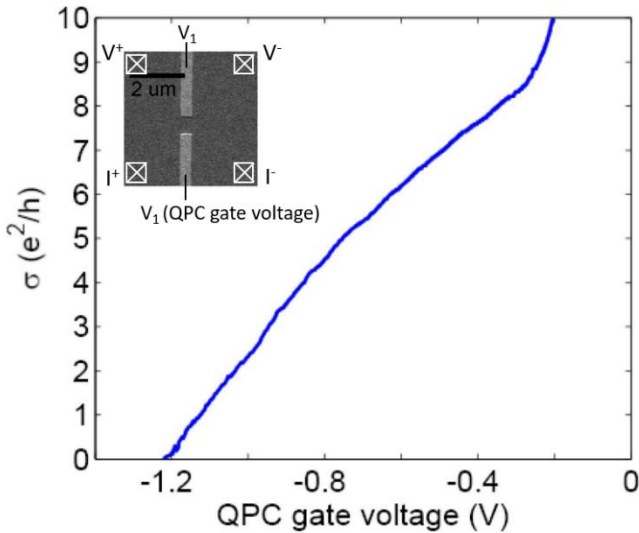
Figure 3. The conductance as a function of gate voltage of a quantum point contact fabricated over a GaAs/AlGaAs heterostructure hosting a two-dimensional electron gas measured on our probe. The measurement was performed at 2 Kelvin. The carrier density in the two dimensional electron gas was 1.2×10^{11} cm^{-2}. The inset shows a scanning electron micrograph of a device different than the one measured but with a similar device geometry.

Noise reduction by shielding wires from chamber ground

In addition to preventing device failure from ESD our probe allows measurement leads to be shielded from the PPMS chamber. We observed an improved signal to noise ratio when the probe was connected to an analog ground provided by a voltage pre-amplifier compared to when the probe is connected to the PPMS ground. Figure 4A,B shows the voltage output from a voltage pre-amplifier measuring the voltage over a 1 kΩ resistor under an AC excitation of 1 nA at a frequency of 13.371 Hz. The voltage pre-amplifier gain was 100.
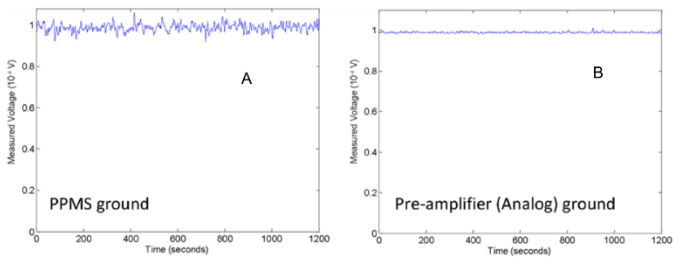

Figure 4. The voltage output from a voltage pre-amplifier measuring the voltage across a 1 kΩ resistor under an AC excitation of 1 nA at a frequency of 13.371 Hz when the probe is connected to PPMS ground (A) and when the probe is connected to the pre-amplifier (analog) ground (B). The voltage pre-amplifier gain was 100, hence the average voltage reported is 10^{-4} V = (1 nA)*(1 kΩ)*(100). The measurement was performed at 2 Kelvin. The large noise in (4A) is also due to single-ended current source being used for the measurement, see discussion in next section.
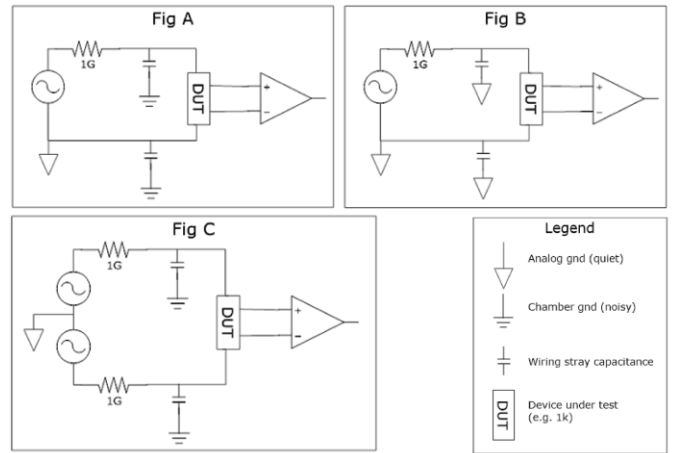

Figure 5. Circuit diagrams showing various grounding and measurement scenarios. Measurements in this app note are single-ended (A and B), while QD measurements are typically symmetrically driven (C). Diagrams A and B correspond to data in Fig. 4A and 4B, respectively.

To understand the observed noise in transport data, one must look at the measurement circuit in the context of the system's noise sources. In this note, we focus on capacitive coupling to the noisy chamber ground. The current source used for collecting data in Figure 4 is a single-ended voltage source, referenced to analog ground, and combined in this example with a 1GΩ series resistance (see Figure 5A). It is the simplest current source design and is valid for low impedance samples (DUTs). We assume the voltage measurement is differential, but even if it is single ended (measuring V+ with respect to analog ground), the following arguments would still apply. In this scenario of Figure 5A, the user's probe (Figure 1) is grounded to the PPMS chamber, so we indicate a capacitive coupling from the wiring to the chamber ground. Now consider how noise from that ground couples into our circuit. Looking back into the source the plus side has an impedance of 1GΩ, but the minus side has very low impedance (it is just a wire to ground). Voltage noise is created by the currents from capacitive coupling multiplied by the impedance back to the source. As a result, the plus side will get a lot of voltage noise coupled into it, but the minus side will get very little. The measured signal (V+) – (V-) will therefore be noisy. See figure 4A for an example of this noise level. As an aside, when DUT resistance is small one may choose to reduce the source impedance (say to 100 MΩ) which will proportionately reduce the noise voltage.

Figure 5B corresponds to the device grounding described in this app note, which replaces chamber ground with quiet analog ground for the wiring stray capacitance. The ground is quiet, so much less noise couples into the amplifier (see Figure 4B).

Figure 5C shows another architecture: a measurement in which the source is driven symmetrically with respect to ground and the amplifier is differential, also positioned symmetrically about ground (here we allow ourselves to use the noisy chamber wiring to illustrate our point). For the noise issue at hand, the important part is that the source **impedance** is symmetric. Since both plus and minus lines get the same chamber voltage fluctuations coupled into them, the differential amplifier cancels them out! (For completeness:

cancellation is true only up to common mode rejection performance of the amplifier.) This symmetric architecture is used in all of Quantum Design's transport measurement electronics: AC Transport, DC Resistivity, and ETO. In practice, QD electronics typically use true current sources, but that doesn't change the noise rejection properties. It just replaces the 1G resistors with a higher impedance. This symmetric circuit design thus enables the QD measurement options to make nanovolt sensitive measurements using the chamber wiring.

So, which setup is best? Probably the ultimate noise performance would come from Figure 5C but with wiring stray capacitance to quiet analog ground. But fully symmetric drives and amplifiers take considerable effort to get right, and are often not available off-the-shelf for customizable measurements. So for anything designed from scratch in the lab, Figure 5B may be the most practical. In addition to the noise benefits, it provides:

- Overvoltage protection for sensitive devices
- Lower common mode noise. QD amplifiers reject this very well, but this will not be the case for all third party electronics. Also, some measurements types, such as gating and tunneling, may actually be sensitive to common mode noise.
- Ability to choose which part of the device is at ground potential, which is useful for gating applications.